

block diagram of 702. (See the specification, paragraph [0036].) In paragraph [0030], the specification expressly states that the circuit 702 (and hence the further examples of circuit 702 shown in Figure 8) "illustrates a block diagram of a processing circuit 702 that may be located partially or entirely on one or more daughter cards such as those illustrated in Figures 4A-4E and 6A-6E." Thus, Figures 7 and 8 show electric circuits that are disposed on daughter cards. Therefore, the objection to the drawings should be withdrawn.

Claim 1 has been objected to on the grounds that "test" in "semiconductor test apparatus" should be "tester." Applicants do not understand why "test" is considered improper in the phrase "semiconductor test apparatus." The apparatus described is for testing semiconductors; hence, "semiconductor test apparatus" is an accurate description. Therefore, the objection to claim 1 should be withdrawn.

① Several claims are rejected under 35 USC § 112, second paragraph as indefinite on the grounds that the term "electric circuit" is not clear. Applicants traverse this rejection. The term "electric circuit" is commonly used and sufficiently well understood by persons of ordinary skill in the field to render the claims definite. Therefore, the rejection under § 112 should be withdrawn.

All of the claims have been rejected as unpatentable over the admitted prior art shown in Figure 3B. Applicants traverse this rejection.

② Independent claims 1, 19, and 50 specify that the daughter card is secured to the substrate "in space relationship." Item 104 of Figure 3B, which the PTO equates with the daughter card of claim 1, is not in a spaced relationship with the item 102 of Figure 3B, which the PTO equates with the substrate of claim 1. That is, there is no space between items 102 and 104 in Figure 3B and hence no spaced relationship between items 102 and 104. Therefore, Figure 3B does not anticipate independent claims 1, 19, and 50.

Moreover, nothing in Figure 3B suggests moving item 104 such that it is spaced from the PCB 102. Indeed, the specification described item 104 of Figure 3B as a mechanism for attaching the probe head assembly 106 to the printed circuit board 102. (See specification, last sentence of paragraph [0003].) Thus, item 104 is essentially a clamp for clamping probe head assembly 106 to the PCB 102, and there is simply no reason to provide a space between a clamp and the PCB 102. Therefore, Figure 3B fails to render obvious independent claims 1, 19, and 50.

(2) Independent claims 42 and 50 and dependent claims 2 and 20 require that at least a portion of an electric circuit be disposed on the daughter card. The PTO equates processing circuitry 302 in Figure 3B with the electric circuit of claims 42, 50, 2, and 20, and the PTO equates mechanism 104 with the daughter card of claims 42, 50, 2, and 20. The processing circuitry 302 shown in Figure 3B, however, is clearly not disposed on the mechanism 104, but is disposed on the printed circuit board 102. Therefore, Figure 3B does not anticipate independent claims 42 and 50 and dependent claims 2 and 20.

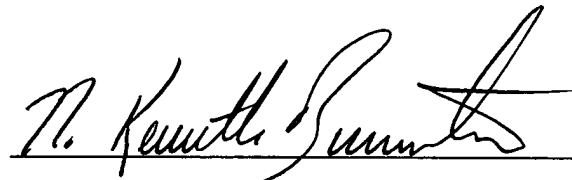
Moreover, nothing in Figure 3B suggests moving any part of processing circuitry 302 to mechanism 104. As discussed above, the specification describes item 104 of Figure 3B as a mechanism for attaching the probe head assembly 106 to the printed circuit board 102. (See specification, last sentence of paragraph [0003].) Thus, item 104 is essentially a clamp. There is simply no reason to move any part of processing circuitry 302 to a clamp 104. Indeed, there is not reason to suppose that one could dispose processing circuitry on a clamp. Therefore, Figure 3B fails to render obvious independent claims 42 and 50 and dependent claims 2 and 20.

Although Applicants believe that all necessary extensions of time and fees have been provided for in papers filed with this Amendment, Applicants petition the Director for any extension of time deemed necessary for acceptance of this paper, and Applicants authorize the Director to charge any fee deemed necessary for acceptance of this paper to Deposit Account No. 50-0285 (order no. P136-US).

Respectfully submitted,

Date: January 28, 2003

By:



N. Kenneth Burraston
Registration No. 39,923

FormFactor, Inc.
Legal Department
2140 Research Dr.
Livermore, CA 94550
925-456-3915
925-294-8147 Fax